WHAT IS CLAIMED IS:

1. A semiconductor memory device capable of simultaneously reading data and refreshing data, comprising:

a data inputting circuit for receiving data inputted from an external circuit;

a parity generating circuit for generating parity data from the data input from said data inputting circuit;

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit;

a refreshing circuit for refreshing said memory;

a reading circuit for reading the data from said memory;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit; and

a parity outputting circuit for directly reading and outputting the parity data stored in said memory.

2. A semiconductor memory device according to claim 1, wherein said parity outputting circuit outputs the parity data via a terminal which is the same as a terminal through which said data outputting circuit outputs data.

3. A semiconductor memory device capable of simultaneously reading data and refreshing data, comprising:

a data inputting circuit for receiving data inputted from an external circuit;

a parity generating circuit for generating parity data from the data input from said data inputting circuit;

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit;

a refreshing circuit for refreshing said memory;

a reading circuit for reading the data from said memory;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit; and

a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity data is stored.

4. A semiconductor memory device according to claim 3, wherein said writing circuit inputs said desired data via a terminal which is the same as a terminal through which said data inputting circuit inputs data.

5. A semiconductor memory device according to claim 3, further comprising a parity outputting circuit for reading and directly outputting said parity data stored in said memory.

6. A semiconductor memory device capable of simultaneously reading data and refreshing data, comprising:

a data inputting circuit for receiving data inputted from an external circuit;

a parity generating circuit for generating parity data from the data input from said data inputting circuit;

a memory for storing the data input from said data inputting circuit and the parity data generated by said parity generating circuit;

a refreshing circuit for refreshing said memory;

a reading circuit for reading the data from said memory;

a restoring circuit for restoring data to be refreshed by said refreshing circuit from other data read normally and corresponding parity data, while said reading circuit is reading data;

a data outputting circuit for outputting the data read by said reading circuit and the data restored by said restoring circuit; and

a control circuit for controlling said refreshing circuit to refresh a given area according to a request from an external circuit.

7. A semiconductor memory device according to claim 6, wherein said control circuit disables refreshing operation on all areas of said memory, and said data outputting circuit outputs data which is not restored based on parity data.

8. A semiconductor memory device according to claim 6, wherein said control circuit controls said refreshing circuit to refresh an area specified by the external circuit, and said data outputting circuit outputs data read from said area to be refreshed and restored based on parity data.

9. A semiconductor memory device according to claim 6, further comprising a writing circuit for directly writing desired data supplied from an external circuit in an area of said memory where said parity data is stored, and said control circuit controls said refreshing circuit to refresh an area specified by the external circuit.